

~~Add A1~~

- a plurality of input channels allocated to the plesiochronous signals, the input channels being connected to a clock synchronizer for adapting the received plesiochronous signals to a common processing clock, and

2. The circuit arrangement of Claim 1 wherein the clock synchronizer contains a plurality of buffer memories corresponding to the plurality of input channels for writing in the signals with their plesiochronous signal clock, and for reading out the signals with a synchronous processing clock.

4. A circuit arrangement for a transmission part of an SDH transmission system for transmitting plesiochronous signals, comprising

a desynchronizer following the transmission processing means for recovery of the plesiochronous signal clocks of the plesiochronous signals and to issue the plesiochronous signals to a plurality of output channels.

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